REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 2-3 are presently active in this case, Claim 1 having been canceled without prejudice and Claims 2 and 3 amended by the present amendment. No new matter has been added. Claims 4-6 have been withdrawn from consideration as drawn to a non-elected invention.

In the outstanding Office Action, Claims 1 and 3 were objected to for informalities; Claim 1 was rejected under 35 U.S.C. § 102(b) as anticipated by Gardner, et al. (U.S. Patent No. 5,863,824, herein "Gardner"); Claim 2 was rejected under 35 U.S.C. § 103(a) as unpatentable over Gardner in view of Aronowitz, et al. (U.S. Patent No. 5,877,530, herein "Aronowitz"); and Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner in view of Xiang, et al. (U.S. Patent No. 6,703,648, herein "Xiang").

Applicant and Applicant's representative wish to thank Examiner Huynh for the interview granted on June 15, 2004. During that interview, the outstanding rejections were discussed in detail. Further, during the interview amended claims along the lines presented herewith were discussed and arguments as hereinafter discussed were presented. During the interview Examiner Huynh indicated that he would further consider the amended claims when such amended claims are formally presented in a filed response.

In regard to Claim 1, Claim 1 has been canceled, thereby rendering the objection and rejection of Claim 1 moot. In regard to the objection to Claim 3, Claim 3 has been amended to correct the noted informalities. Accordingly, Applicant respectfully requests that the objection be withdrawn.

Applicant respectfully traverses the rejection of Claim 2 under 35 U.S.C. § 103(a) as unpatentable over Gardner in view of Aronowitz for the following reasons.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be demonstrated. First, Gardner in view of Aronowitz must teach or suggest each and every element recited in the claim.[1] Second, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention.[2] Third, a reasonable probability of success must exist with respect to the proposed combination relied upon in the rejection.[3]

Amended Claim 1 recites a semiconductor device comprising, a plurality of gate electrode structures formed on a semiconductor substrate, wherein respective lengths in the plurality of gate electrode structures are substantially uniform with one another, each of said lengths being defined as a sum of a gate length extending on an interface between a gate insulating film and the gate electrode, and a width of an offset spacer extending on an interface between the offset spacer and a semiconductor substrate, and the plurality of gate electrode structures include a first gate electrode having a rectangular section, a second gate electrode having an upwardly tapered section, and a third gate electrode having a downwardly tapered section.

The outstanding Office Action asserts that Gardner in view of Aronowitz teach or suggest each and every element recited in Claim 2. Applicant respectfully disagrees.

Gardner discloses,

> [t]he present invention relates to a method of producing a semiconductor device with transistors having controlled drive current strength. Consistent with the present invention, a semiconductor device is formed by

[1] See MPEP § 2143.
[2] Id.
[3] Id

> forming a gate electrode over a substrate. The length of the gate electrode is measured and compared to a desired design length. A spacer is formed on the gate electrode. The size of the spacer is determined, based on the difference between the measured and designed length of the gate electrode layer. Thus, the spacer can be varied to take into account the variation in gate electrode length from the desired value. This allows the drive current strength of the final semiconductor device to be controlled and also permits variations within and between lots of the semiconductor devices to be reduced. The spacer can be formed in multiple steps to provide even greater flexibility and accuracy.[4]

In regard to Gardner's teaching of measuring the "length of the gate electrode," Gardner teaches,

> The transistor width may, for example, be the length of the polysilicon gate electrode over its respective active area.[5]

Gardner further teaches,

> After the gate electrode 203 has been formed, its dimensions, particularly the length, are measured. For the purposes of this application, the "length" l of the gate electrode will be used to define the dimension of the gate electrode 203 in the direction parallel to the channel. This measurement can be carried out, for example, with a scanning electron microscope. The measurement may be carried out in situ after formation of the gate electrode 203, or the substrate could be transferred to a separate measuring station for measurement if desired.
>
> A single gate electrode on a given substrate can be measured as reflecting the relative variation of gate electrode length from the desired value for all gate electrodes on that substrate. It also would be possible to measure any desired number of electrodes on a given substrate. A single substrate within a batch can be measured as reflecting the relative variation of gate electrode length from the desired value for all of the substrates being processed in that production batch. It also would be possible to measure any desired number, or even all, of the substrates in a given production batch.[6]

From the noted teachings provided by Gardner, it is clear that Gardner does not recognize the existence of gate electrodes having different tapers, as claimed, since Gardner determines the gate electrode width based on a measurement from a scanning tunneling

[4] Gardner, column 2, lines 13-33.

microscope, which presumably would be sensitive to the uppermost gate electrode dimension, and in any event would not be effective to measure a gate electrode length of a gate electrode having a downwardly tapered section in which the dimension of the gate electrode at the interface with the gate insulating film is smaller that the dimension at the top surface of the gate electrode.

Thus, it is respectfully submitted that Gardner does not teach or suggest a plurality of gate electrode structures formed on a semiconductor substrate wherein respective lengths of the plurality of gate electrode structures are substantially uniform with one another, each of said lengths being defined as a sum of a gate length extending on an interface between a gate insulating film and the gate electrode, and a width of an offset spacer extending on an interface between the offset spacer and a semiconductor substrate, and the plurality of gate electrode structures include a first gate electrode having a rectangular section, a second gate electrode having an upwardly tapered section, and a third gate electrode having a downwardly tapered section.

In particular, Applicants respectfully submit that Gardner does not recognize or disclose that a gate electrode may have a rectangular section, an upwardly tapered section, or a downwardly tapered section.[7] In the absence of such a teaching, Gardner fails to teach or suggest the claimed semiconductor device including a plurality of gate electrode structures formed on a semiconductor substrate wherein respective lengths, defined as a sum of a gate length extending on an interface between a gate insulating film and the gate electrode, and a width of an offset spacer extending on an interface between the offset spacer and a semiconductor substrate, of the plurality of gate electrode structures are substantially uniform with one another, wherein the plurality of gate electrode structures include a first gate

[5] Id. column 3, lines 21-23.

electrode having a rectangular section, a second gate electrode having an upwardly tapered section, and a third gate electrode having a downwardly tapered section, as recited in amended Claim 2.

Aronowitz does cure the deficiencies of Gardner. For example, even assuming arguendo Aronowitz is properly combinable with Gardner, which Applicants dispute, Aronowitz does not recognize that a plurality of gate electrode structures formed on a semiconductor substrate may include a first gate electrode having a rectangular section, a second gate electrode having an upwardly tapered section, and a third gate electrode having a downwardly tapered section, either. Accordingly, Aronowitz likewise does not teach or suggest that the length of a gate electrode structure is to be defined by the width of the gate electrode at the interface with the gate insulating film, and the applied references whether considered alone or in combination fail to teach a semiconductor device have a substantially uniform gate structure, regardless of gate electrode taper, as claimed.

Accordingly, Applicants respectfully submit that Claim 2 is patentable and the rejection of Claim 2 under 35 U.S.C. § 103(a) should be withdrawn.

Applicant respectfully traverses the rejection of Claim 3 under 35 U.S.C. § 103(a) as unpatentable over Gardner in view of Xiang on the basis that Xiang fails to cure the deficiencies of Gardner above noted.

In view of the foregoing remarks, it is respectfully submitted that each of Claims 2 and 3 define patentable subject matter, and that the application is in condition for

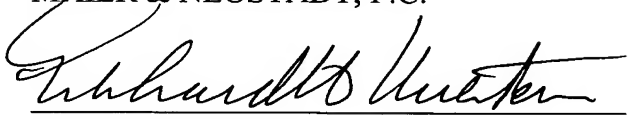
---

[6] Id., column 3, line 56 – column 4, line 8.
[7] See Office Action, page 5.

allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)